VERY LARGE SCALE INTEGRATION (VLSI) ENGINEERING

Post-Graduate Certificate Program

UC SANTA CRUZ SILICON VALLEY CAMPUS
UCSC Silicon Valley Extension

in partnership with EC Higher Education

UCSC Silicon Valley Extension's VLSI (Very Large Scale Integration) Engineering certificate program is the most complete integrated circuit curriculum available in Silicon Valley. Students gain practical experience using the latest EDA tools on Linux in our stateof the-art VLSI Lab. Our expert faculty teaches hardware specification, logic design, verification, synthesis, physical implementation, circuit design, and testing of integrated circuit products.

Who Should Attend?

- Those looking to acquire skills in different areas of VLSI Engineering which helps them grow expertise and advance in their careers
- Experienced technical professionals looking to fill in gaps of knowledge on their jobs or to expand their careers
- Entry-level engineers can acquire hands-on knowledge in VLSI development while networking with fellow students and teaching staff

Prerequisites

A degree in a technical field or equivalent knowledge acquired through training and experience in hardware design and development.

Curriculum

Certificate & OPT | 3 Quarters | 28.5 Units

Devloping the Nanometer ASIC: From Spec to Silicon | 2 Units
This course covers each step in developing an ASIC, explaining key concepts such as transistor action, standard cells, RTL synthesis, meeting timing, functional coverage, formal equivalence, physical design, signal integrity, DFT and BIST, tape-out, IC fabrication, and emerging packaging trends. The course includes hands-on "quick tour" labs to familiarize you with the use of EDA tools. The focus is on mostly-digital ASICs with multiple IP cores, low-power goals, and on-chip RF-CMOS/analog blocks.

Practical Design with Xilinx FPGAs | 3 Units
The course places an architectural focus on the Virtex-7, Artix and Kintex families, as well as the Zynq programmable system on a chip. In-class demonstrations and student design projects will feature the Xilinx Vivado Webpack design software. By the end of the course, you should be able to complete practical designs with Xilinx FPGAs and understand design and timing reports. The course includes a student project with design tools; real device implementation or programming is optional.

Digital Logic Design Using Verilog | 3 Units
This course will prepare you to implement Verilog modeling of digital logic. You will learn Verilog constructs and hardware modeling techniques, Verilog language elements and data types. You will tackle key challenges and learn structural, dataflow and behavioral modeling in Verilog, including common constructs and coding considerations. The instructor includes coding and testing examples of combinational circuits (gates, mux/demux, encoders/decoders, and Boolean expression), sequential circuits (latches, flip-flops, shift registers, counters, RAMs and ROMs), and complex logic (flavors of ALU and FSM).

Linux, Introduction | 2.5 Units
This course introduces the Linux operating system. Linux is gaining popularity on personal computers, devices, embedded systems and enterprise servers. The course gives students an opportunity to use Linux for personal or professional purposes. Students will learn basic Linux administration, Linux file and directory structure, basic network configuration, shell programming and various utilities available in Linux.

Physical Design Flow from Netlist to GDS-II | 3 Units
This course is an introduction to ASIC physical design flow and tools from netlist to GDS-II. The course starts with floor planning and block pin assignment. The instructor then addresses placement and clocktree synthesis, followed by routing, and post-route optimization. You will learn RC extraction, static timing analysis, and physical verification. Upon completion of the course, you will possess the essential knowledge and hands-on

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Curriculum continued

experience with the back-end physical design flows, from a synthesized netlist all the way to layout completion for ASIC chip tapeout.

Logic Synthesis, Introduction | 3 Units
This course outlines various concepts of logic synthesis. Starting with the basics of synthesis, the course explains the Synopsys tools and their use in synthesizing high-level language into gates. It also covers various options such as partitioning, design, gate-level optimization, time/area constraints and library management. The course is intended for design engineers with some knowledge of hardware description languages such as Verilog HDL or VHDL. It is a lab-based course with hands-on exercises.

Low-Power Design of Nano-Scale Digital Circuits | 3 Units
This course introduces advanced topics in nano-scale (below 90nm) VLSI device and circuit design. Highperformance and low-power design issues in modern and future nano-scale CMOS technologies are discussed in detail. You will learn low-power design approaches and techniques at different levels of abstraction. New design techniques are introduced to deal with nano circuit designs under excessive leakage and process variations. You'll also explore several non-classical CMOS devices for circuit design in such technologies, and review prospects of future non-silicon nanotechnologies.

System Verilog for ASIC and FPGA Design | 3 Units
This course prepares hardware engineers, ASIC and FPGA designers, and design-support staff to use the high-level syntax of SystemVerilog to design, debug, and synthesize digital logic for ASICs, FPGAs, and IP cores. You'll learn SystemVerilog's basic building blocks and language constructs, including synthesizable data types and operators, structures and unions, 2-D arrays and loops, and the bus interface unit. In lab sessions, you will write code and synthesize it into digital logic and bus fabric, using both ASIC and FPGA tools.

Mixed-Signal Design | 3 Units
This course will help you understand basic analog circuits and systems, and problems encountered when analog circuits share substrate with digital circuits. You will also learn precautionary measures and techniques used to circumvent these problems. Topics include MOS transistors, basic analog building blocks, phase-locked-loop circuits, sample and hold circuits, comparator design, A/D and D/A converters, and layout considerations in mixed-signal circuits. The course is intended for practicing engineers and design managers who want to understand analog circuit and layout techniques in mixed-signal IC design.

System Verilog Essentials: Functiuonal Verification and Simulation | 3 Units
This lab course introduces the digital simulation process with hands-on exercises using the simulation tool. The instructor discusses simulation techniques such as coding style, event ordering, delta cycle debugging, zero width glitch, race conditions, time slices, conditional compilation, simulation performance and code coverage. SystemVerilog essentials include new data types, interfaces, classes, randomization, and overview of assertions. The course offers examples to show how these tools help designers with code compaction and system verifications.

Internships (unpaid) | 3 Units
Minimum 90 Hours Per Quarter
Enrolling in a certificate program allows you to participate in multiple unpaid internships at local companies in your field of study. Internships are available across a variety of sectors, generally at mid-sized companies, such as Agylytyx, Crowdera Inc, Innowest, and YMedia Labs. Good internships are much sought after and highly competitive. To stand the best chance of securing your preferred placement, our Internship Coordinators are on hand with expert support and guidance.

Courses in the certificate programs are subject to change based on schedule availability and/or student aptitude. Equivalent course substitutions will be made to accommodate.